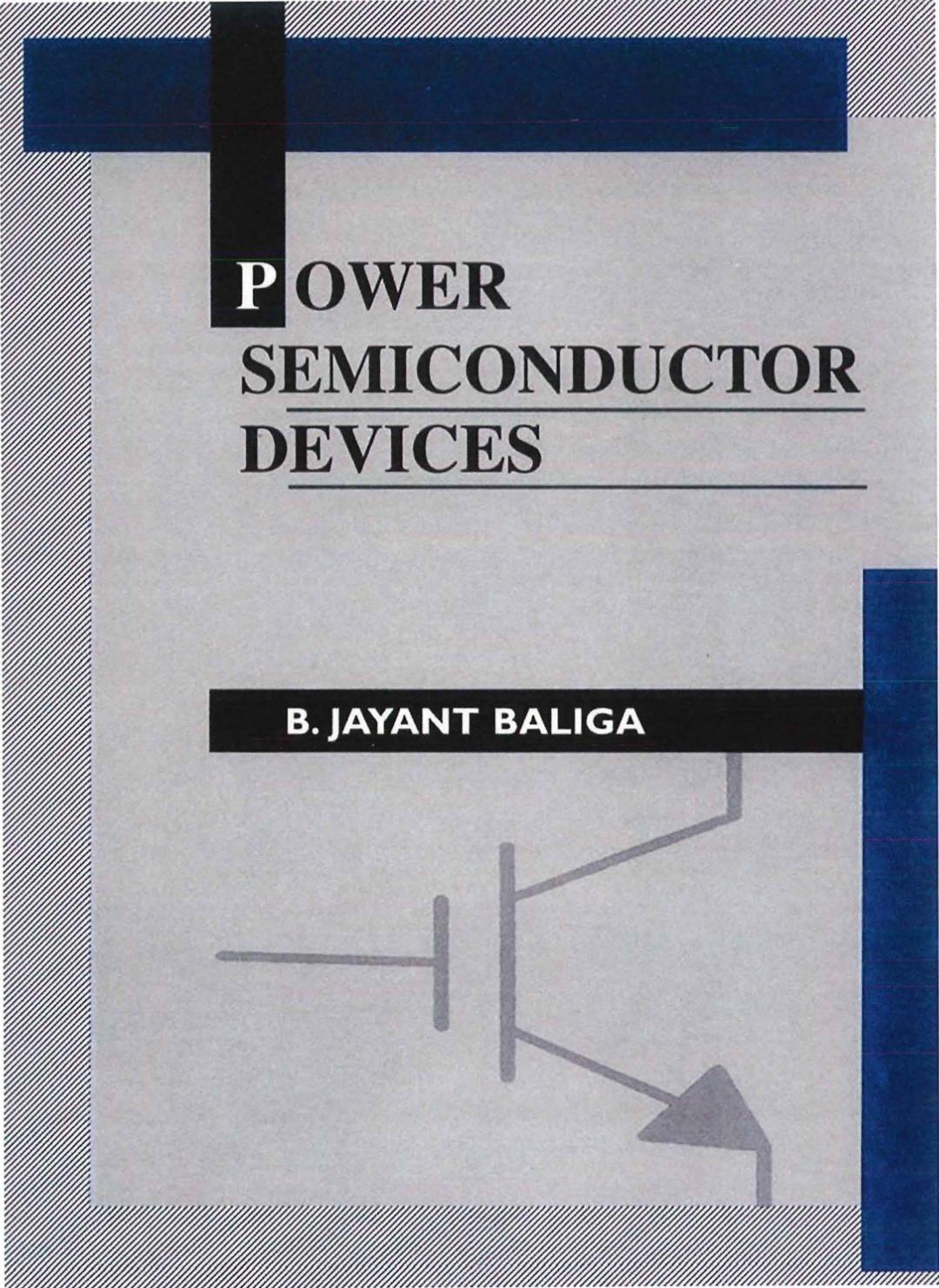
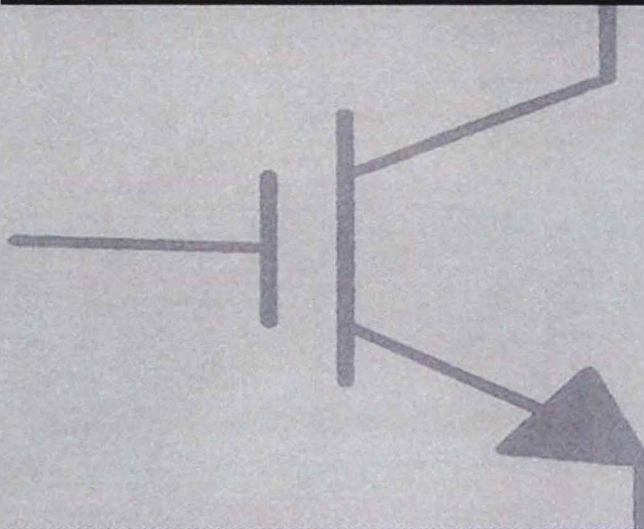


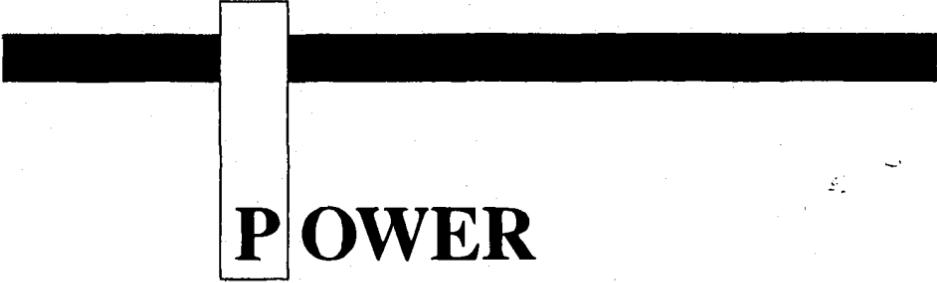
EXHIBIT B



POWER
SEMICONDUCTOR
DEVICES

B. JAYANT BALIGA





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B. JAYANT BALIGA

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This expression is valid even in the presence of a work function difference and oxide charge because these parameters are not strongly affected by the temperature. The bulk potential (Ψ_B) varies with temperature because the energy gap changes with temperature:

$$\frac{d\Psi_B}{dT} = \frac{1}{T} \left[\frac{E_g(T=0)}{2q} - |\Psi_B(T)| \right] \quad (7.131)$$

From these expressions, the rate of variation of the threshold voltage with temperature can be calculated as a function of the background doping level and oxide thickness. Note that the threshold voltage will vary at a higher rate for thicker gate oxides and higher substrate doping levels. During the design and fabrication of power MOSFETs, it is important to provide an adequate room temperature threshold voltage that will allow operation at high temperatures with sufficient margin to ensure noise immunity and protection from inadvertent turn-on when a high $[dV/dt]$ is applied.

7.10 DEVICE STRUCTURES AND TECHNOLOGY

Two fundamentally different processes have evolved for the fabrication of discrete vertical channel power MOSFETs. One of these processes relies upon the planar diffusion of the P-base and N^+ emitter from a common window defined by the refractory gate electrode to form the DMOS structure shown in Fig. 7.2, while the other process utilizes reactive ion etching of the silicon surface to form the U-groove structure shown in Fig. 7.3. Due to the poor performance of the V-groove power MOSFET structure shown in Fig. 7.1, its process will not be discussed. The discussion here will be confined to the case of n-channel devices. The fabrication of complementary (p-channel) devices is similar.

7.10.1 DMOS (Planar) Structure

For the fabrication of the planar power MOSFET structure shown in Fig. 7.2, the wafer orientation can be chosen to provide the highest surface mobility in order to achieve a low channel contribution to the on-resistance. For this reason, these devices are fabricated using (100) oriented wafers. Due to the extremely rapid increase in on-resistance with increasing breakdown voltage, power MOSFETs are confined to blocking voltages of less than 1,000 volts. The ideal depletion width for these devices is less than 100 microns. They must be fabricated by growing lightly doped epitaxial layers (typically 5 to 50 microns thick) on heavily doped substrates. In the case of n-channel devices, the N^+ substrates are antimony doped with a resistivity of 0.01 ohm-cm. Antimony is chosen as the dopant because its autodoping effects are small during epitaxial growth. For low on-resistance devices, arsenic doped substrates with a resistivity of 0.001 ohm-cm are preferred.

After epitaxial growth, a thick field oxide is grown. This oxide is patterned to create the

desired planar diffused edge termination. Sometimes the processing of the diffusion for the edge termination is combined with the DMOS cell fabrication. Following the termination diffusion, the device active area (central region where the DMOS cells are to be fabricated) is opened up. The gate oxide is then grown to a typical thickness of 1,000 Å. Recently device manufacturers have been scaling down the gate oxide thickness to obtain an increase in the transconductance so as to make it possible to drive the power MOSFETs at voltages compatible with low voltage logic circuits.

A layer of heavily doped polysilicon (or other refractory gate material) is now deposited. After oxidizing the polysilicon, a photomasking step is used to pattern the polysilicon to the surface of the gate oxide. A cross-section of a small segment of the active region is shown at

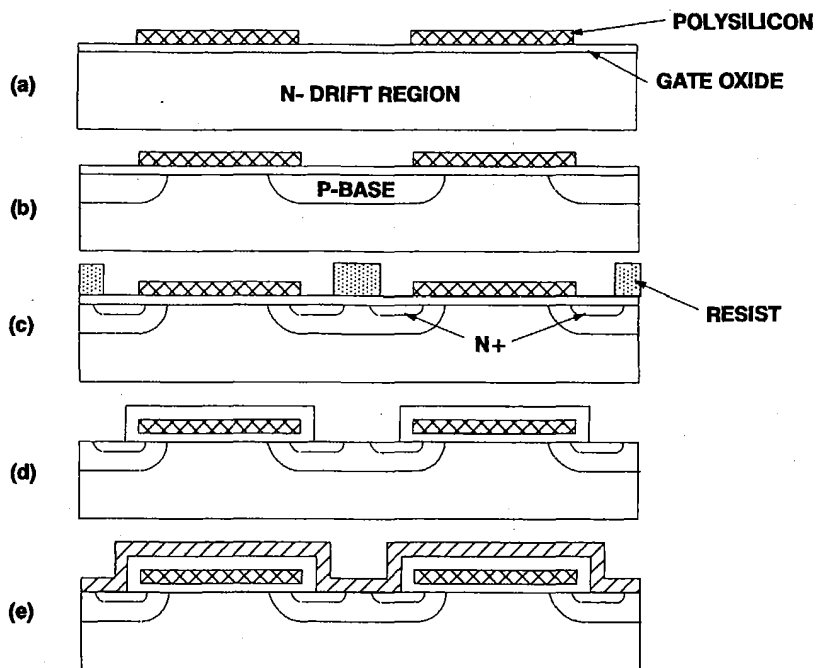


Fig. 7.53 Process sequence used to make the power DMOSFET structure.

this point in the process in Fig. 7.53(a). At this point in the process, the cell window has been defined. Boron is now implanted through the gate oxide to a dose (typically 10^{14} per cm^2) that is necessary to obtain the desired threshold voltage in conjunction with the N^+ emitter diffusion. The boron is driven-in with a wet oxidation step to obtain the structure shown in Fig. 7.53(b). An oxide island is now patterned at the center of each cell window to mask the N^+ emitter diffusion. This oxide island leaves a portion of the P-base accessible at the surface in each cell allowing good contacts to be subsequently made to it.

The patterning of the oxide island is one of the critical alignment steps during the DMOS process. If the oxide island is misaligned with respect to the edges of the polysilicon in the cell window, the length of the N^+ emitter will increase, causing degradation of the $[dV/dt]$ and safe-operating-area. After the oxide island is formed, the N^+ emitter is diffused either by using phosphorus predeposition or by ion implantation. The latter process provides greater control over the emitter profile and threshold voltage. A typical dose is 1×10^{15} per cm^2 . The device cross-section at this point is shown in Fig. 7.53(c). After the N^+ emitter is diffused, a thick layer of oxide is deposited by using low pressure chemical vapor deposition (LPCVD). This provides a conformal insulating film over the top and sides of the polysilicon gate electrode.

The oxide layer is now patterned to form the contact windows as illustrated in Fig. 7.53(d). This is another critical photolithographic step in the DMOS process because misalignment can either cause poor contact to the P-base region or lead to an overlap of the contact with the polysilicon at the cell edges. This overlap will produce a short between source and gate. The final step in the device process consists of metallization to create the structure shown in Fig. 7.53(e). The DMOS process described here provides the fundamental basis for the fabrication of modern power MOSFETs. Many variations of the process have been explored in an attempt either to eliminate some of the critical alignment steps or to provide self-alignment of the N^+ emitter and contact windows.

7.10.2 U MOS Structure

As in the case of the DMOS process, the U MOS process begins with the growth of a lightly doped N-type epitaxial layer on an N^+ substrate. After the growth and patterning of a thick field oxide, a boron diffusion is performed to create a P-base region across the entire active area of the device and to form the multiple field ring edge termination. The oxide layer grown during the P-base diffusion step is next patterned to define windows for the source region, and an N^+ implant is performed followed by its drive-in step. A cross-section of the active region at this point in the process is shown in Fig. 7.54(a). Note that, in this process, the N^+ source region extends across the entire top surface of the mesa region. The contact to the P-base region is made at selected locations along the length of the fingers orthogonal to the cross-section shown in Fig. 7.54.

A silicon nitride layer is now deposited on the top surface with a thin oxide buffer layer. This nitride layer is used later in the process to allow selective oxidation of the trench sidewalls. A thick oxide layer is deposited on top of the nitride layer to act as a mask during the reactive ion etching step used to form the trenches. This oxide/nitride stack is patterned using the third mask to define windows where the trenches are to be formed. Reactive ion etching is performed using conditions that favor the formation of vertically walled trenches. An example of such an etch is SF_6 mixed with oxygen. This method has been shown to not only produce vertical sidewalls but to also create a rounded bottom for the trench. This reduces the high electric field normally observed at the corners of the trenches. A cross-section of the active region at this point in the process is shown in Fig. 7.54(b).

A polysilicon layer is now deposited on the wafer using a conformal coating process. The polysilicon will then fill the U-groove formed by the trench etch step and will also cover

high frequencies.

7.11 SILICON CARBIDE POWER MOSFETS

As discussed earlier in this chapter, the specific on-resistance of the silicon power DMOSFET and UMOSFET structures approaches the ideal specific on-resistance of the drift region. Unfortunately, the ideal specific on-resistance for silicon, given by Eq. (7.58), increases rapidly with the breakdown voltage. For breakdown voltages above 200 volts, the ideal specific on-resistance for the n-channel silicon MOSFET becomes greater than 1×10^{-2} ohm-cm². This implies that the on-state voltage drop will exceed 10 volts for an on-state current density of 100 amperes per cm², resulting a very high power dissipation within the devices. Although it is possible to reduce the on-state power loss by decreasing the on-state current density, this is undesirable because of the corresponding increase in device area which leads to higher chip cost.

From a fundamental physics viewpoint, a lower specific on-resistance for the drift layer is achievable if the semiconductor has a higher breakdown electric field strength. Using the basic equation derived in Chapter 3 for an abrupt parallel plane junction, it can be shown that for obtaining a desired breakdown voltage (BV), the drift region must have a doping concentration N_D of:

$$N_D = \frac{\epsilon_s E_c^2}{2 q BV} \quad (7.132)$$

and a thickness W_D of:

$$W_D = \frac{2 BV}{E_c} \quad (7.133)$$

where E_c is the critical electric field at which avalanche breakdown occurs in the semiconductor. The specific on-resistance of the drift region, which was also defined as the ideal specific on-resistance, is then given by:

$$R_{on-sp(ideal)} = \frac{W_D}{q \mu_n N_D} = \frac{4 BV^2}{\epsilon_s E_c^3 \mu_n} \quad (7.134)$$

Thus, the ideal specific on-resistance decreases inversely proportional to the mobility and as the cube of the breakdown electric field strength. The denominator ($\epsilon_s E_c^3 \mu_n$) in Eq. (7.134) has been referred to as *Baliga's figure of merit for unipolar power devices*.

By using the known material properties of semiconductors, it is possible to select those that will exhibit a lower ideal specific on-resistance when compared with silicon by using this expression. It has been found that the most promising semiconductors are gallium arsenide, whose Baliga's figure-of-merit is 12.7 times larger than silicon, and silicon carbide whose

Baliga's figure-of-merit is 200 times larger than silicon. Although some research has been performed on the fabrication of vertical power MESFETs from gallium arsenide, this material has been found to be difficult to work with due to the dissociation of the compound during processing. In contrast, silicon carbide offers a much larger improvement in the ideal specific on-resistance and is stable even at extremely high temperatures.

In terms of the fabrication of silicon carbide based power MOSFETs, there are several outstanding problems that must be overcome. First, the diffusion rates for impurities in silicon carbide are orders of magnitude lower than for silicon. This precludes the possibility for fabrication of the DMOS cell structure using polysilicon as the gate electrode. The UMOS gate structure is more amenable to fabrication if the P-base and N^+ source regions are epitaxially grown. As discussed earlier in this chapter, the UMOS gate structure also offers a substantial increase in the channel density, which reduces the channel resistance contribution. In spite of this, calculations of the specific on-resistance of silicon carbide power UMOSFETs indicate very high contributions from the channel resistance resulting from the low electron inversion layer mobilities reported in the literature. This indicates that silicon carbide power MOSFETs would not be competitive with silicon devices unless the breakdown voltages exceed 1000 volts.

This problem can be overcome by using a new power switch configuration, called the *Baliga-pair*, which, as shown in Fig. 7.56, consists of a silicon power MOSFET connected in series with the source region of a silicon carbide high voltage power MESFET (which has a

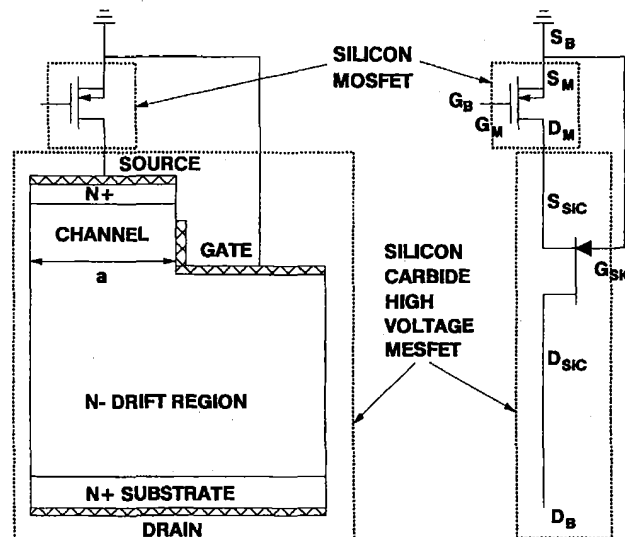


Fig. 7.56 The *Baliga-pair* power switch configuration.

Schottky barrier gate structure) or JFET (which has a P-N junction gate structure). Although a vertical channel trench-gate MESFET structure is illustrated in this figure, a lateral device could instead be used. It is important to note that the gate region of the silicon carbide

MESFET is connected to the reference terminal (or source region of the silicon power MOSFET) and that the composite switch is controlled by a signal applied to the gate of the silicon power MOSFET. The basic operating principles of this switch are discussed below.

If the half-width 'a' of the MESFET channel is designed to be larger than the zero bias depletion width of the MESFET gate structure, the MESFET will behave as a depletion-mode (or normally-on) device structure. If an increasing positive bias is applied to the drain D_B of the Baliga-pair with the gate G_B shorted to the source S_B , the voltage will be initially supported by the silicon MOSFET because the MESFET channel is not depleted. This will result in an increase in the potential of the source region S_{SiC} of the silicon carbide MESFET. Since the gate G_{SiC} of the silicon carbide MESFET is at zero potential, this will produce a reverse bias across the gate-source junction of the MESFET. As the voltage applied to the drain D_B is increased, this reverse bias will produce a pinch-off of the MESFET channel by the extension of a depletion region from the gate contact. Once the MESFET channel pinches-off, any further increase in the voltage applied to the drain D_B will be supported by the extension of a depletion region in the drift region of the silicon carbide MESFET. It has been shown by two-dimensional numerical simulations that, once the channel is pinched-off, the potential at the drain D_M of the MOSFET remains relatively constant and independent of the voltage applied to the drain D_B of the composite switch. Since a channel pinch-off voltage of less than 25 volts can be easily designed, this implies that a silicon power MOSFET with relatively low breakdown voltage can be used in conjunction with a high voltage silicon carbide MESFET to form the Baliga-pair.

This is important from the point of view of obtaining a low total on-state voltage drop for the composite switch. In order to turn on the Baliga-pair, a positive gate bias is applied to the gate G_M of the silicon power MOSFET, which also serves as the gate G_B of the composite switch. This switches the silicon MOSFET to its highly conductive state. When a positive voltage is applied to the drain D_B , current can now flow through the undepleted MESFET channel and the silicon MOSFET. The simulations have demonstrated that the specific on-resistance of the silicon carbide MESFET is very close to the ideal specific on-resistance for the drift region because of a uniform current distribution in the drift region. The resistance contribution from the MESFET channel increases the specific on-resistance by less than 25 percent because the current is transported in the bulk and not along a surface. Thus, the Baliga-pair is projected to have on-state voltage drops of only 0.1 volt when the MESFET is designed to block up to 1000 volts.

The Baliga-pair has several other important attributes. The first is an excellent forward biased safe operating area (FBSOA). This is achieved by simply reducing the gate bias applied to the switch until it approaches the threshold voltage for the silicon power MOSFET. In this case, when a voltage is applied to the drain D_B , the MOSFET operates in its current saturation regime. This limits the current flowing through the composite switch. When the voltage applied to the drain D_B is increased, the voltage across the MOSFET increases until the channel of the MESFET is pinched-off, allowing high voltages to be sustained with a current flow dictated by the MOSFET channel. The numerical simulations indicate a square FBSOA for the Baliga-pair because no minority carrier transport is involved.

The absence of minority carrier transport in the Baliga-pair is also important in obtaining a high switching speed. Since both the silicon MOSFET and the silicon carbide MESFET are unipolar devices, the turn-off time for the composite switch is determined by the charging and

discharging time constants for the silicon MOSFET. Well optimized silicon power MOSFETs can be designed at the required low breakdown voltages, resulting in a very high switching speed for the Baliga-pair. This is attractive for the reduction of power losses in medium/high voltage power electronics systems operating at high frequencies.

Another attribute of the Baliga-pair is that it incorporates an excellent integral flyback diode. In the case of the silicon power MOSFET, it was shown in Section 7.8 that the junction between the P-base region and the N-drift region can be utilized as a reverse conducting (flyback) diode. However, this diode operates with the injection of minority carriers into the drift region, which compromises the switching speed and power losses in the devices. In the case of the silicon carbide MOSFET structure, there is an additional disadvantage that the potential required for the injection of minority carriers is much larger (typically 3 volts) when compared with silicon (typically 1 volt) due to its larger energy band gap. This results in a severe increase in the power losses for the flyback rectifier. In contrast to this, in the case of the Baliga-pair, the application of a negative bias to the drain D_g forward biases the Schottky barrier gate structure. As discussed in Chapter 4 on power rectifiers, the silicon carbide Schottky barrier rectifier has been demonstrated to have excellent on-state and switching characteristics because it is a unipolar device. Thus, the Baliga-pair also contains an excellent flyback diode if implemented by using a high voltage silicon carbide MESFET structure.

The basic operation of the Baliga-pair has been verified by using silicon power MOSFETs and silicon high voltage vertical channel JFETs. The implementation of this switch with silicon carbide devices awaits the successful fabrication of silicon carbide MESFET structures with high breakdown voltages.

7.12 TRENDS

Power MOSFETs have the following attributes: (a) a voltage controlled characteristic with low input gate power, (b) a stable negative temperature coefficient for the on-resistance, (c) a wide safe-operating-area, and (d) a high switching speed. Due to these features, when first introduced, the devices were expected to replace power bipolar transistors in many applications. This has occurred for systems with low operating voltages. Examples are switch-mode power supplies, computer peripherals, and automotive electronics. This displacement has not occurred for systems operating at high voltages due to the high on-resistance of power MOSFETs designed to support voltages above 200 volts. With rapid progress along the learning curve, the manufacturing cost of power MOSFETs now rivals that for the bipolar transistors. Since the on-resistance of the silicon power MOSFETs is already close to the ideal value, progress in increasing their power handling capability can be achieved only by increasing the area of the device. This is expected to occur by a pace dictated by improvements in process technology that lead to a reduction in defect density. Recently, it has been theoretically shown that replacement of silicon with silicon carbide would lead to a 200 fold reduction in the specific on-resistance. This offers a tremendous opportunity for improvement of device characteristics if the technological problems with manufacturing silicon carbide devices can be overcome.